1. An imaging device formed as an integrated circuit comprising:

a photosensitive device for accumulating photo-generated charge in an underlying portion of a semiconductor substrate; and

a readout circuit comprising at least an output transistor;

wherein said imaging device is in a row of similar imaging devices in an array and shares a column output line with an adjacent imaging device of the row.

2. The imaging device according to claim 1, wherein said photosensitive device is selected from the group consisting of a photogate, a photodiode and a photoconductor.

3. The imaging device according to claim 1, wherein said photosensitive device includes a photodiode.

4. The imaging device according to claim 1, wherein said photosensitive device includes a photoconductor.

5. The imaging device according to claim 1, wherein said photosensitive device includes an active area for accumulating photo-generated charge having a generally diagonally shaped component.

6. The imaging device according to claim 1, further comprising a controllable charge transfer region having a control terminal, said transfer region being formed in said substrate adjacent said photosensitive area and having a node connected to a gate of said output transistor and at least one charge

transfer device for transferring charge from said photosensitive area to said node in accordance with a control signal applied to said control terminal.

7. The imaging device according to claim 6, wherein said charge transfer device is a field effect transistor.

8. The imaging device according to claim 1, further comprising a straight column line formed of a metal layer in an integrated circuit to address said imaging device.

9. The imaging device according to claim 6, further comprising a reset transistor for resetting said node in response to a reset signal.

10. The imaging device according to claim 9, wherein said reset transistor is addressed by a reset line which is linear in said substrate.

11. The imaging device according to claim 10, wherein said reset line is formed of a material selected from the group consisting of doped polysilicon, metals and refractory metal silicides.

12. The imaging device according to claim 10, further comprising a row select transistor responsive to a row select signal to activate said imaging device.

13. The imaging device according to claim 12, wherein said row select transistor is addressed by a row select line which is linear in said substrate.

14. The imaging device according to claim 13, wherein said row select line is formed of a material selected from the group consisting of doped polysilicon, metals, refractory metal silicides and mixtures thereof.

15. A method for generating an output signal corresponding to an image focused on a sensor array having rows and columns of pixel sensors wherein two adjacent pixel sensors in a row are connected to a shared column line, each sensor capable of collecting electrical charge based on a detected light intensity, the method comprising the steps of:

activating a first sensor in a row connected to a shared column line for a first period of time then subsequently activating an adjacent second sensors in the row connected to said shared column line for a second period of time.

16. The method for generating an output signal according to claim 15, further comprising:

detecting a first voltage at a node of a respective activated sensor;

resetting the voltage of the respective nodes of said activated sensors to a predetermined reset voltage, wherein said voltage is reset by a reset transistor;

transferring electrical charges collected by said activated sensor to said node;

detecting a second voltage at said node; and

generating an output signal over said shared column line.

17. The method for generating an output signal according to claim 15, wherein said sensor is selected from the group consisting of a photogate, a photodiode and a photoconductor.

18. The method for generating an output signal according to claim 15, wherein said node is a floating diffusion node.

19. The method for generating an output signal according to claim 15, wherein said shared column line is formed of a metal layer.

20. The method for generating an output signal according to claim 15, wherein said shared column line is linear in said substrate.

21. The method for generating an output signal according to claim 16, wherein said reset transistor is addressed by a reset line which is linear in said substrate.

22. The method for generating an output signal according to claim 21, wherein said reset line is formed of a material selected from the group consisting of doped polysilicon, metals, refractory metal silicides and mixtures thereof.

23. The method for generating an output signal according to claim 16, wherein said row select transistor is addressed by a row select line which is linear in said substrate.

24. The method for generating an output signal according to claim 23, wherein said row select line is formed of a material selected from the group consisting of doped polysilicon, metals, refractory metal silicides and mixtures thereof.

25. An imaging system comprising:

a plurality of pixel cells having an active sensor area which includes a diagonally shaped component, the cells being arranged into an array of rows and columns, each pixel cell being operable to generate a voltage at a diffusion node corresponding to detected light intensity by the sensor, wherein two cells in a row share a common column line for addressing said pixel cell and the pixel cells

in the row that share the common column line are alternatively addressed by respective row select lines.

26. The imaging system according to claim 25, further comprising:

a reset device to reset the voltage of a diffusion node formed in the cells;

a transfer device to transfer charge from said pixel cells to said diffusion node;

a row select device connected to either said odd row select line or said even row select line respectively;

a row decoder having a plurality of control lines connected to the pixel cells, each control line being connected to the cells in contact with a respective column, wherein the row decoder is operable to activate the odd cells in said rows and said even cells in said rows by said row select device; and

a plurality of output circuits respectively connected to a pixel cell, each output circuit being operable to store a voltage signal received from a respective pixel cell and to provide a sensor output signal.

27. The imaging system according to claim 25, wherein said pixel cells include a photogate, a photodiode or a photoconductor in said active area.

28. The imaging system according to claim 26, wherein the diffusion node is a floating diffusion node.

29. The imaging system according to claim 25, wherein said column line addressing two adjacent rows of pixel cells is linear in said substrate.

30. The imaging device according to claim 29, wherein said column line is formed of a metal.

31. The imaging system according to claim 26, wherein said reset device is addressed by a reset line which is linear in said substrate.

32. The imaging system according to claim 31, wherein said reset line is formed of a material selected from the group consisting of doped polysilicon, metals, refractory metal silicides and mixtures thereof.

33. The imaging system according to claim 26, wherein said row select device is addressed by a row select line which is linear in said substrate.

34. The imaging system according to claim 33, wherein said row select line is formed of a material selected from the group consisting of doped polysilicon, metals, refractory metal silicides and mixtures thereof.

35. A CMOS imager array comprising:

a plurality of CMOS imager pixels for generating an output signal from detected light and arranged in rows and columns in an array;

a plurality of column lines each connected to at least two adjacent pixels of a row in said array, said column lines being connected to output circuitry to output signals generated from detected light;

a plurality of odd row select lines orthogonal to said column lines to address odd pixels in said rows;

a plurality of even row select lines orthogonal to said column lines to address even pixels in said rows;

column drivers to address the pixels connected to said column lines;

row drivers to address the pixels through said odd row lines and said even row lines.

36. The CMOS imager array according to claim 35, wherein said plurality of CMOS imager pixels have an active area having a diagonally shaped component.

37. The CMOS imager array according to claim 35, wherein said column line is linear in said array.

38. The CMOS imager array according to claim 36, wherein said column line is formed of a metal.

39. The CMOS imager array according to claim 35, wherein said odd row lines and said even row lines are is linear in said array.

40. The CMOS imager array according to claim 38, wherein said odd and even row select lines are formed of materials selected from the group consisting of doped polysilicon, metals, refractory metal silicides and mixtures thereof.

41. A system comprising:

(i) a processor; and

(ii) a CMOS imaging device coupled to said processor and including:

a photosensitive device for accumulating photo-generated charge in an underlying portion of a semiconductor substrate; and

a readout circuit comprising at least an output transistor;

wherein said imaging device is in a row of similar imaging devices in an array and shares a column output line with an adjacent imaging device of the row.

42. The system according to claim 41, wherein said photosensitive device selected from the group consisting of a photogate, a photodiode and a photoconductor.

43. The system according to claim 41, wherein said photosensitive device includes an active area for accumulating photo-generated charge having a generally diagonally shaped component.

44. The system according to claim 41, further comprising a controllable charge transfer region having a control terminal, said transfer region being formed in said substrate adjacent said photosensitive area and having a node connected to a gate of said output transistor and at least one charge transfer device for transferring charge from said photosensitive area to said node in accordance with a control signal applied to said control terminal.

45. The system according to claim 44, wherein said charge transfer device is a field effect transistor.

46. The system according to claim 41, further comprising a straight column line formed of a metal layer in a substrate to address said imaging device.

47. The system according to claim 44, further comprising a reset transistor for resetting said node in response to a reset signal.

48. The system according to claim 47, wherein said reset transistor is addressed by a reset line which is linear in said substrate.

49. The system according to claim 48, wherein said reset line is formed of a material selected from the group consisting of doped polysilicon, metals, refractory metal silicides and mixtures thereof.

50. The system according to claim 48, further comprising a row select transistor responsive to a row select signal to activate said imaging device.

51. The system according to claim 50, wherein said row select transistor is addressed by a row select line which is linear in said substrate.

52. The system according to claim 51, wherein said row select line is formed of a material selected from the group consisting of doped polysilicon, metals, refractory metal silicides and mixtures thereof.

53. The system according to claim 41, wherein the photosensitve area of said imaging devices sharing a column line is generally S-shaped.

54. The system according to claim 41, wherein said system is a camera system.

55. The system according to claim 41, wherein said system is a scanner.

56. The system according to claim 41, wherein said system is a machine vision system.

57. The system according to claim 41, wherein said system is a vehicle navigation system.

58. The system according to claim 41, wherein said system is a video telephone system.